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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/790,986
Filing Date: March 02, 2004
Appellant(s): EGUCHI, TAKEO

Takeo Eguchi
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07/22/2009 appealing from the Office action mailed 11/24/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,272,648	Agrawal et al.	6-1981
2001/0025292 A1	Denk et al.	9-2001

The Admitted Prior Art in pages 1-5 of the present Application.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. Whether claims 1-4, 9-13 and 17-20 are patentable under 35 U.S.C. 103(a) in view of U.S. Patent No. 4,272,648 to Agrawal et al. and U.S. Patent Publication No. 2001/0025292 to Denk et al.

B. Whether claims 14-16 are patentable under 35 U.S.C. 103(a) in view of U.S. Patent No. 4,272,648 to Agrawal et al., U.S. Patent Publication No. 2001/0025292 to Denk et al. and the Admitted Prior Art.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 9-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al. (U.S. 4,272,648) in view of Denk et al. (U.S. 2001/0025292 A1).

Re claim 1, Agrawal et al. disclose in Figures 1-5 a signal processing apparatus (e.g. Figure 1) for receiving digital signals that are continuously related and input sequentially (e.g. after sampling and digitized by components 19 and 23 in Figure 1), performing a predetermined operation on each of sequentially input digital signals (e.g. Figures 3-5 as typical operations), and outputting a result of the operation (e.g. output of Figures 3-5 to the next operation), the signal processing apparatus (e.g. Figure 1) comprising: operation means for performing the predetermined operation on an input digital signal (e.g. multiplication process as seen in Figure 3 prior reducing word length); high-order part extraction means for extracting a necessary high-order part by rounding off a result of the operation performed by the operation means (e.g. component 63 in Figure 3); difference calculation means for calculating the difference between the result of the operation performed by the operation means and the high-order part extracted by the high-order part extraction means (e.g. component 64 in Figure 3); and feedback means for adding, to a next input digital signal, the difference value calculated by the difference calculation means or a value obtained by performing a predetermined operation on the difference value calculated by the difference calculation means (e.g. feedback as seen in Figure 3 wherein the error is feedback to the adder 62 through delay element 65 to the next sample).

Agrawal et al. fail to disclose the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value. However, Denk et al.

disclose in Figures 1-17 the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value (e.g. component 840 in Figure 8 and paragraphs [0035-0040]).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value as seen in Denk et al.'s invention into Agrawal et al.'s invention because it would enable to minimize or eliminate error in reducing wordlength (e.g. paragraph [0009]).

Re claim 2, Agrawal et al. further disclose in Figures 1-5 a second set of continuously-related digital signals is sequentially input after completion of inputting of a first set of continuously-related digital signals (e.g. next sample is fed continuously into the system), a difference value obtained as a result of the difference calculation performed (e.g. error signal obtained by adder 64), by the difference calculation means, on the last digital signal of the first set of digital signals or a value obtained by performing the predetermined operation on the difference value calculated by the difference means is reset to 0 or added with a particular value (e.g. most significant digital of error is either 0 or error signal from adder 64 in Figure 3), and the resultant value is added, via the feedback means, to the first digital signal of the second digital signals (e.g. by adder 62 in Figure 3).

Re claim 3, Agrawal et al. further disclose in Figures 1-5 feedback means adds, to the next input digital signal, a value obtained by multiplying the difference value calculated by the difference calculation means by a factor smaller than 1 (e.g. only the

most significant digit of error signal e(N), technically the error signal is scaled down by N-1 digits as seen in Figure 3).

Re claim 4, Agrawal et al. further disclose in Figures 1-5 a digital signal acquired by means of over sampling is input to the operation means (e.g. Figure 5).

Re claim 9, it is a medium claim of claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, it is a medium claim having similar limitations cited in claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 11, it is a medium claim having similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it is a medium claim having similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it is a method claim having similar limitations cited in claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, Agrawal et al. fail to disclose in Figures 1-5 the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure. However, Denk et al. disclose in Figures

1-17 the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure (e.g. Figure 9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure as seen in Denk et al.'s invention into Agrawal et al.'s invention because it would enable to minimize or eliminate error in reducing wordlength (e.g. paragraph [0009]).

Re claims 18-20, Agrawal et al. fail to disclose in Figures 1-5 an error is produced during the rounding off and the error is capable of being input to one of the high-order part extraction means and a low-order part extraction means depending on a factor; if an error is equal to or greater than a factor, then the error is input to the high-order part extraction means, and if the error is less than the factor, then the error is input to a low-order part extraction means; and an error is produced if the result is not rounded up and is calculated via the difference calculation means and added to a next input digital signal via the feedback means. However, Denk et al. disclose in Figures 1-17 an error is produced during the rounding off and the error is capable of being input to one of the high-order part extraction means and a low-order part extraction means depending on a factor (e.g. Figure 9 wherein the factor is the threshold and bias factor); if an error is equal to or greater than a factor, then the error is input to the high-order part extraction means, and if the error is less than the factor, then the error is input to a low-order part extraction means (e.g. Figures 7-9 with the condition comparison with threshold value); and an error is

produced if the result is not rounded up and is calculated via the difference calculation means and added to a next input digital signal via the feedback means (e.g. inherently exists in Figures 7-9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an error is produced during the rounding off and the error is capable of being input to one of the high-order part extraction means and a low-order part extraction means depending on a factor; if an error is equal to or greater than a factor, then the error is input to the high-order part extraction means, and if the error is less than the factor, then the error is input to a low-order part extraction means; and an error is produced if the result is not rounded up and is calculated via the difference calculation means and added to a next input digital signal via the feedback means as seen in Denk et al.'s invention into Agrawal et al.'s invention because it would enable to minimize or eliminate error in reducing wordlength (e.g. paragraph [0009]).

3. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al. (U.S. 4,272,648) in view of Denk et al. (U.S. 2001/0025292 A1), as applied to claim 1 above, and in further view of the admitted prior art.

Re claims 14-15, Agrawal et al. fail to disclose low-order part extraction means for extracting a necessary low-order part by rounding off the result of the operation performed by the operation means; wherein the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value as if a lower-order value output from the lower-order part extraction means is equal to or greater than a

predetermined factor, the lower-order value is rounded up to a high-order value and added to an output of the high-order part extraction means. However, Denk et al. disclose in Figures 1-17 the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value (e.g. component 840 in Figure 8 and paragraphs [0035-0040]). Further, the admitted prior art discloses low-order part extraction means for extracting a necessary low-order part by rounding off the result of the operation performed by the operation means as if a lower-order value output from the lower-order part extraction means is equal to or greater than a predetermined factor, the lower-order value is rounded up to a high-order value and added to an output of the high-order part extraction means (e.g. pages 2-3).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add low-order part extraction means for extracting a necessary low-order part by rounding off the result of the operation performed by the operation means; wherein the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value as if a lower-order value output from the lower-order part extraction means is equal to or greater than a predetermined factor, the lower-order value is rounded up to a high-order value and added to an output of the high-order part extraction means as seen in Denk et al.'s invention and the admitted prior art into Agrawal et al.'s invention because it would reduce error in average (e.g. page 3 lines 10-13 and paragraph [0009]).

Re claim 16, Agrawal et al. fail to disclose the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded

resultant is less than a predetermined figure. However, the admitted prior art discloses the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure (e.g. pages 2-3).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure as seen in the admitted prior art into Agrawal et al.'s invention because it would enable to reduce error in average (e.g. page 3 lines 10-13).

(10) Response to Argument

A. Whether claims 1-4, 9-13 and 17-20 are patentable under 35 U.S.C. 103(a) in view of U.S. Patent No. 4,272,648 to Agrawal et al. and U.S. Patent Publication No. 2001/0025292 to Denk et al. [Pages 7-9]

The applicant argues in pages 7-8, particularly last two paragraphs in page 7, for independent claims 1, 9 and 13 that Agrawal et al. and Denk et al. cannot be combined without destroying the intended purpose of Agrawal et al., and in any event, Denk et al. teaches away from Agrawal et al. since Agrawal et al. supports to provide increased accuracy with respect to gain control by truncating or chopping off a portion of a number and adding the truncated portion to another number wherein Denk et al. disclose an apparatus and method for reducing precision of data.

The examiner respectfully submits that combination of references by Argawal et al. (primary) and Denk et al. (secondary) would not destroying the intended purpose of

the primary reference by Argawal et al. as alleged by the applicant, but rather the combination or the use of secondary reference by Denk et al. would improve the intended purpose by reducing/eliminating error during truncating or chopping-off process in the primary reference. For example, the truncating or chopping-off of input 5.39 would be 5.3 with 0.09 error wherein the rounding (e.g. up or to nearest value) of input 5.39 would be 5.4 with 0.01 error. In addition, nothing within the secondary reference by Denk et al. would expressively or inherently prohibit the combination of references.

Further, the applicant has mis-understood the conception of "reducing precision of data" as part of rounding process, but rather the conception of "reducing precision of data" is the overall architecture of the invention which reducing the input data size from X (size m) to X' (size [m-n]). Reducing the input data size is also reducing precision of input data which has nothing to do the rounding process. The rounding process would actually improve the reduced precision input data by either minimized or eliminated rounding error as clearly disclosed within many passages including the abstract and summary of the invention. For instant, let input to be 10 digits X= {5426.849248} and the output to be 5 digits X^c = {5426.84} and X' = {5426.85} wherein X is the input data; X^c is called "reducing precision of input data" without rounding and X' is called "reducing precision of input data" with rounding. As you can see X' is improve version of X^c by rounding process.

Generally, it is very obvious and reasonable for combining the references by Argawal et al. and Denk et al. since both disclose same field of endeavor which reducing the input data width/size however Denk et al. further introduce the rounding processes

(e.g. nearest value) which would minimize or eliminate the rounding error. Thus, it would yield a predictable improved result of reducing wordlength/size/width.

The applicant further argues in pages 8-9, particularly last paragraph in page 8, for claims 1, 9 and 13 that the logic for combining would be flawed for at least three reasons: (1) the provided passage from Denk et al. fails to provide any nexus between "rounding" and the remaining disclosure in Denk et al.; (2) it is nonsensical to use Denk's rounding to "minimize or eliminate error" because the rounding does exactly the opposite by creating a less accurate result; (3) one would view rounding as problematic and would never apply to chopping-off process since Denk discloses the passage of "in this manner, errors due to rounding are minimized or eliminated".

The examiner respectfully submits that the logic for combining the references is very obvious and reasonable instead of flaw as alleged by the applicant since:

(1) it is unclear in the argument why the provided passages from Denk et al. must provide some nexus between "rounding" and the remaining disclosure in Denk et al. as argued by the applicant. Even if there is a requirement, the reference by Denk et al., as whole, clearly provide nexus between "rounding" and the remaining disclosure, particularly Figure 3. The rounding process is applied to the reduced wordlength/size/width of input data X' to yield an improved result hat(X) of the reduced precision X' as clearly seen in Figure 3;

(2) "Rounding" process does not create a less accurate result as alleged by the applicant. "Rounding" (to nearest) is an improvement of chopping-off or truncation as

known in http://en.wikipedia.org/wiki/Round-off_error. It is nowhere within the reference by Denk et al. would clearly point-out that the rounding does exactly the opposite of chopping-off or truncation by creating a less accurate result. As detail in the previous responses, the applicant has mis-understood the conception of "reducing precision of data" as part of rounding process, but rather the conception of "reducing precision of data" is the overall architecture of the invention which reducing the input data size from X (size m) to X' (size [m-n]). Reducing the input data size is also reducing precision of input data which has nothing to do the rounding process. The rounding process would actually improve the reduced precision input data by either minimized or eliminated rounding error as clearly disclosed within many passages including the abstract and summary of the invention. For instant, let input to be 10 digits X= {5426.849248} and the output to be 5 digits X^c = {5426.84} and X' = {5426.85} wherein X is the input data; X^c is called "reducing precision of input data" without rounding and X' is called "reducing precision of input data" with rounding. As you can see X' is improve version of X^c by rounding process; and

(3) One would not view the rounding process as problematic over the chopping-off process as alleged by the applicant since chopping-off would introduce error due to losing the chopped-off significant bits wherein rounding process would minimize or eliminate the error. Thus, it is very obvious and reasonable for combining the references by Argawal et al. and Denk et al. since both disclose same field of endeavor which reducing the input data width/size however Denk et al. further introduce the rounding

processes (e.g. nearest value) which would minimize or eliminate the rounding error. Thus, it would yield a predictable improved result of reducing wordlength/size/width.

B. Whether claims 14-16 are patentable under 35 U.S.C. 103(a) in view of U.S. Patent No. 4,272,648 to Agrawal et al., U.S. Patent Publication No. 2001/0025292 to Denk et al. and the Admitted Prior Art. [Pages 9-11]

The applicant further argues in pages 9-11, with exact argument as seen in the above Part A, for claims 14-16 rejected under 35 U.S.C. 103(a) in view of Agrawal et al. and Denk et al. and further in view of the Admitted Prior Art that the combination would destroy the intended purpose and the combination would be flawed due to there reasons as listed above.

The examiner respectfully submits that the same above responses can also apply here since the applicant repeats the exact argument as above. In general, the combination of references by Argawal et al. (primary) and Denk et al. (secondary) would not destroying the intended purpose of the primary reference by Argawal et al. as alleged by the applicant, but rather the combination or the use of secondary reference by Denk et al. would improve the intended purpose by reducing/eliminating error during truncating or chopping-off process in the primary reference. For example, the truncating or chopping-off of input 5.39 would be 5.3 with 0.09 error wherein the rounding (e.g. up or to nearest value) of input 5.39 would be 5.4 with 0.01 error. In addition, nothing within the secondary reference by Denk et al. would expressively or inherently prohibit the combination of references.

Further, the applicant has mis-understood the conception of "reducing precision of data" as part of rounding process, but rather the conception of "reducing precision of data" is the overall architecture of the invention which reducing the input data size from X (size m) to X' (size [m-n]). Reducing the input data size is also reducing precision of input data which has nothing to do the rounding process. The rounding process would actually improve the reduced precision input data by either minimized or eliminated rounding error as clearly disclosed within many passages including the abstract and summary of the invention. For instant, let input to be 10 digits X= {5426.849248} and the output to be 5 digits X^c = {5426.84} and X' = {5426.85} wherein X is the input data; X^c is called "reducing precision of input data" without rounding and X' is called "reducing precision of input data" with rounding. As you can see X' is improve version of X^c by rounding process. Further, "Rounding" process does not create a less accurate result as alleged by the applicant. "Rounding" (to nearest) is an improvement of chopping-off or truncation as known in http://en.wikipedia.org/wiki/Round-off_error. It is nowhere within the reference by Denk et al. would clearly point-out that the rounding does exactly the opposite of chopping-off or truncation by creating a less accurate result. As detail in the previous responses, the applicant has mis-understood the conception of "reducing precision of data" as part of rounding process, but rather the conception of "reducing precision of data" is the overall architecture of the invention which reducing the input data size from X (size m) to X' (size [m-n]). Reducing the input data size is also reducing precision of input data which has nothing to do the rounding process. The rounding process would actually improve the reduced precision input data by either

minimized or eliminated rounding error as clearly disclosed within many passages including the abstract and summary of the invention. For instant, let input to be 10 digits X= {5426.849248} and the output to be 5 digits X^c = {5426.84} and X' = {5426.85} wherein X is the input data; X^c is called "reducing precision of input data" without rounding and X' is called "reducing precision of input data" with rounding. As you can see X' is improve version of X^c by rounding process.

Generally, it is very obvious and reasonable for combining the references by Argawal et al. and Denk et al. since both disclose same field of endeavor which reducing the input data width/size however Denk et al. further introduce the rounding processes (e.g. nearest value) which would minimize or eliminate the rounding error. Thus, it would yield a predictable improved result of reducing wordlength/size/width.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Chat C. Do/

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